Analysis of topologies of MOSFET Current Mirrors

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***Abstract*—Current mirrors are circuits widely used in microelectronics, especially in analog IC design. They have as a principle the generation of a replica of the reference current at the output node. This paper aims to conduct a comparative study on different topologies of NMOS current mirrors, specifically the Simple Current Mirror, the Cascode Current Mirror, and the Wilson Current Mirror. We analyze their electrical characteristics concerning the channel width (W) of the transistors and operating temperature. The Cadence Virtuoso was used as a simulation tool, and the target process technology was 130 nm. As a result, we found that by increasing the W of the transistors the minimum output voltage decreases. Moreover, we noticed a considered effect of temperature over the output current in the three topologies. Finally, it can be concluded that the current mirrors followed the expected patterns of the main literature and converged in the direction of what represented the main equations that command the MOSFETs transistors.**

***Index Terms*—Cascode current mirror, Simple current mirror, Wilson current mirror.**

I. Introduction

In analog IC design, the current mirror (CM) is an essential circuit and its structure is one of the most commonly used concepts. Current mirrors are simply an extension of the current sink/source and are widely used in analog circuits where current bias is affected by the supply voltage [1] [2].

The CM uses the principle that if the gate-source potentials of two identical MOS transistors are equal, the drain currents should be equal if no second-order effects are considered [3] [4].

The application of current mirrors is wide-ranging and can be found in current amplification, biasing of active loads and level shifting [2] as well as in physiological stimulation [5], current mode signal processing [6] [5] and biomedical applications [7].

Therefore, this paper analyzes three CM topologies: a simple current mirror, a cascode current mirror, and a Wilson current mirror. To analyze the effect of temperature on the current mirrors, we used three different sizes for the channel length (W) of transistors for each topology: 900 nm, 1800 nm, and 2700 nm.

We then performed an analysis of the behavior of the current mirrors by changing the W values of the transistors from 900 nm to 9000 nm. This analysis examined the value of the output voltage where the output current reached 10 uA at a nominal supply voltage of 1.5 V.

It is important to emphasise that in all cases the reference current was fixed at 10 μA and the temperature of the simulation was 27 ºC.

After, we changed the operating temperature to evaluate its effects on the three topologies. For this analysis, the temperature was set to 0 ºC and 70 ºC. The value of the output current was annotated when the voltage of the output node reached the minimum value at a temperature of 27 ºC.

The minimum and maximum output voltages ($V_{out_{min}}$ and $V_{out_{max}}$) are the minimum and maximum voltage values, respectively, that the output node must reach for the current mirror to function properly. These points are called the compliance voltages and define the compliance range, which is the range of the output voltage in which the current mirror will operate properly. We define the compliance range as the output voltage range where the mirrored current is within $I_{ref} \pm 10\%$. We also define the voltage V_1, which is the output voltage that the current mirror produces when $I_{out} = I_{ref}$. Fig. 1 shows an example of how these points are determined. It illustrates the variation of the output current of a current mirror as a function of the output voltage.

II. Current mirror topologies

This section describes the three topologies of current mirrors studied in this work, including their main characteristics and electrical behavior.

A. Simple Current Mirror

The most basic topology of a current mirror is shown in Fig.4. It represents the simplest way to copy the current with MOS transistors. As mentioned earlier, the current mirror is based on the principle that if identical MOS transistors have the same gate-source voltage, their drain currents should also be the same [3]. That is, two identical MOS devices having equal gate-source voltages and operating in saturation will carry equal currents [8]. This is possible because ideally the principle that $I_d = f(V_{GS})$ holds for the MOSFET in the saturation region.

From this fact it can also be concluded that $V_{GS} = f^{-}1(I_d)$. Thus, the current I_{out} in Fig. 4 can be written as a function of I_{ref}, since the V_{GS} of both transistors are equal. Thus, if

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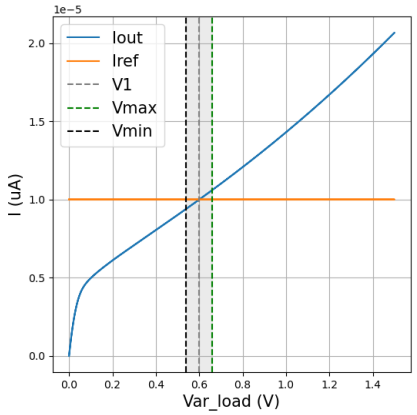


Fig. 1: Determination of V_1, compliance voltage $V_{out_{min}}$ and compliance range.

the gate-source voltage of the reference transistor is replicated to the gate and source terminals of the copy transistor and both transistors have the same dimensions, the current will be $I_{out} = f[f^{-}1(I_{ref})] = I_{ref}$ [8].

However, the above mathematical analysis is valid only if the drain-source voltage V_{DS} of both transistors is the same, otherwise second-order effects, such as the channel length modulation effect, will change the drain current of the mirror transistor. Making both V_{DS} equal is not practical in real circuits, since the output voltage is undefined in the design of a current mirror and may change during the operation of the circuit. This fact leads to an error in the copy current, which, as shown in Eq. 1, must be evaluated.

$$\frac{I_{ref}}{I_{out}} = \left(\frac{L_1 W_2}{W_1 L_2}\right) \cdot \left(\frac{V_{GS2} - V_{T2}}{V_{GS1} - V_{T1}}\right)^2 \cdot \left(\frac{1 + \lambda V_{DS2}}{1 + \lambda V_{DS11}}\right) \quad (1)$$

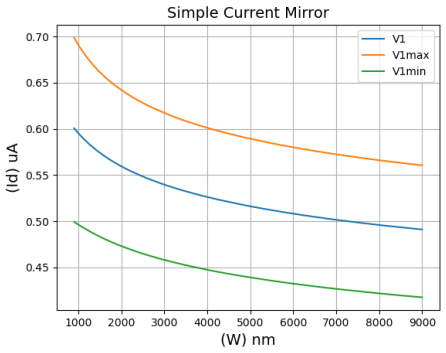
B. Cascode Current Mirror

Another way to copy a current is through the Cascode current mirror, whose schematic is shown in Fig. 6. In practice, the error caused by channel length modulation produces a significant error of the copied current, especially when minimum length transistors are used.

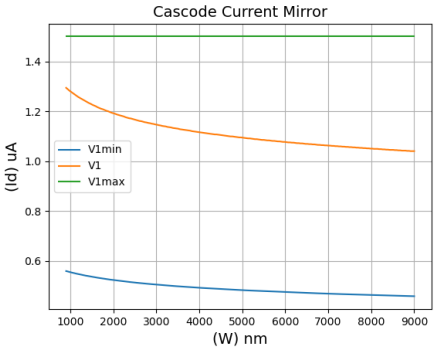
The Cascode current mirror reduces ratio errors due to differences in output and input voltages. Its small-signal output resistance is much greater than that of a simple current mirror. This can be seen from the equations representing the output resistance of both current mirrors. Equation 2 models the output resistance of the simple current mirror and equation 3 models the output resistance of the cascode current mirror, showing that the output resistance of the cascode is larger than that of the simple current mirror [3] [9] [10].

$$rout = \frac{1}{gds} \quad (2)$$

$$rout = rds2 + rds4 + gm4 \cdot rds2 \cdot rds4 \cdot (1 + \eta) \quad (3)$$



(a) Simple Current Mirror



(b) Cascode Current Mirror

Fig. 2: Compliance range for different values of W.

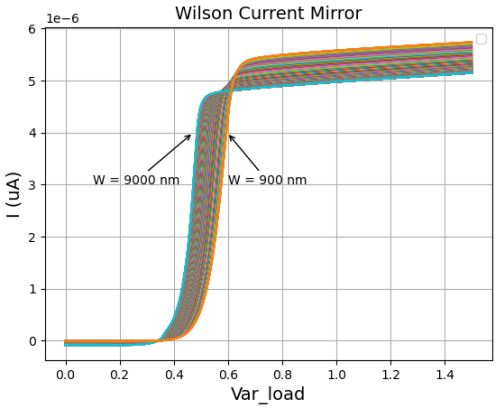


Fig. 3: $Vout$ x $Iout$ for different values of W for the Wilson current mirror.

C. Wilson current mirror

Another topology of the current mirror that provides a more constant output current is the Wilson current mirror, shown in Fig. 7. It provides a much more accurate input to output current gain.

The output resistance of the Wilson current mirror is increased by using negative current feedback. If I_{out} increases, then the current through M2 also increases. The mirror effect of M1 and M2 causes the current in M1 to increase.

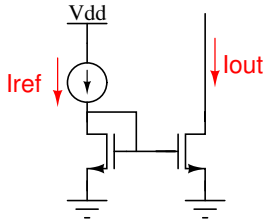
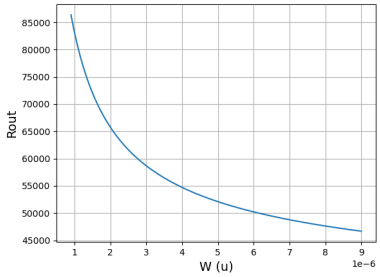
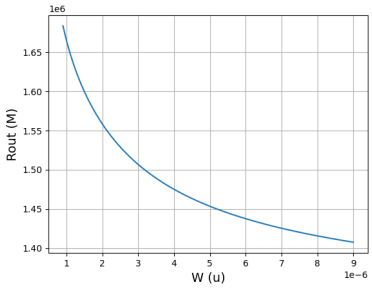


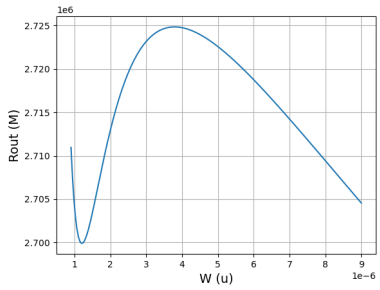
Fig. 4: Simple current mirror.



(a) Rout X W (Simple current mirror).



(b) Rout X W (Cascode current mirror).



(c) Rout X W (Wilson Current Mirror

Fig. 5: Output resistance in function of W for the three topologies of current mirror.

If I_{ref} is constant and we assume that there is some resistance between the gate of M3 (drain of M1) and the ground, the gate voltage of M3 decreases as the current I_{out} increases. This configuration increases the output resistance of the current mirror.

III. Simulation Results

This section presents the electrical simulation results for the experiments performed with the three current mirror topologies studied.

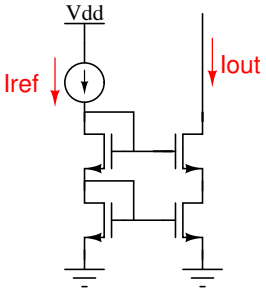


Fig. 6: Cascode current mirror.

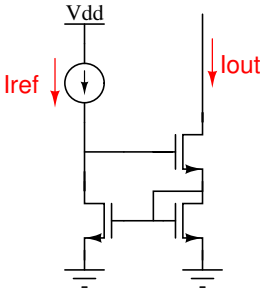


Fig. 7: Wilson current mirror.

It is important to emphasise that the channel length (L) of the MOSFET transistors was fixed at 130 nm in all cases.

In the first round of simulation, a temperature of 27 ºC and a VDD of 1.5 V were used. A sweep of the output voltage from 0 to VDD was considered in the simulation. The voltage values at the output were recorded when the current I_{out} reached exactly 10 μA, indicating the values of V_1. The simulations were repeated for W 900 nm to 9000 nm

After that, we kept VDD at 1.5 V and changed the temperature to 0 ºC and 70 ºC. In this situation, the value of the current I_{out} was extracted at the same V_1 as in the previous cases. For this case, the simulations were repeated for W = 900 nm, 1800 nm and 2700 nm.

A. Load sensitivity

We analyze the effect of load variations on the value of the copied current. Fig.2 shows the case where the transistor W values were changed from 900 nm to 9000 nm, which was applied to the studied current mirrors. For this situation, V_1 represents the voltage when the current $Iout$ reaches 10 μA, in addition to V_1min and V_1max represents the change of $Iout$ in $\pm 10\%$.

An important fact to point out regarding the Wilson current mirror is that it is designed for $I_{out} = I_{ref}/2$, i.e., the expected I_{out} is 5 μA because I_{ref} is 10 μA. Thus, for the Wilson current mirror case, the voltage V_1 was recorded when the current I_{out} reached the value of 5 μA.

It is possible to point out that the Simple Current Mirror has the smaller V_1, but the smaller compliance range.

Choosing V1 with a value of $1V$, one can observe in Fig.5 that the simple current mirror has a $Rout$ that is more sensitive

to the changes of W than the cascode current mirror and the Wilson current mirror. The Cascode Current Mirror, on the other hand, has a larger V_1 and a larger compliance range, along with a larger output resistance.

Another point is that the value of V_1 for the simple current mirror and the Cascode Current Mirror decreases when the value of W is increased. This happens because of the relationship between the current I_{ref} and I_{out} shown in equation 1. Increasing W decreases the value of V_{GS} required to produce the same drain current, and the same happens with the output transistor saturation voltage.

In addition, another compelling fact is highlighted and illustrated in Fig.7, where it is possible to note that with a smaller W, it takes less voltage (V1) to reach the desired $Iout$, in this case of $5uA$, compared to a W of 9000n. The larger the size of the W, the higher the value of V1 to reach 5 μA.

B. I_{out} sensitivity to temperature

Table I shows the case where the temperature at which the current mirrors were simulated is varied. The applied temperature was 27 ºC, 0 ºC, and 70 ºC. In these situations, we observed the value of I_{out} when the output voltage is equal to the value of V_1 obtained in the previous experiment.

When the temperature drops to 0 ºC, a decrease in output current values is observed in all cases. On the other hand, when the temperature increases to 70 ºC, one can see an increase in the output current. This is because the current mirrors are biased with low currents and the values of V_{GS} are close to V_T. The increase in temperature reduces the threshold voltage in MOS transistors, which increases the drain current I_D [11].

IV. Conclusion

The simulation results obtained in this work allowed us to observe the effects of varying the W of the transistors and temperature for three different current mirror topologies. Increasing the channel width of the transistors leads to an improvement in the value of the copied current in all analyses.

Moreover, it can be observed that for the simple and the cascode current mirrors, the value of $Vout$ to reach the desired value of $Iout$ decreases as W is increased. This behaveior was not observed for the Wilson current mirror. In this case, with the increase in the value of W, it was necessary to use a higher value of $Vout$ to achieve the value of $Iout$ = 5μA.

Finally, another important observation concerns the effects of temperature. It is observed that the increase in temperature leads to an increase in the output current with respect to V1. On the other hand, the opposite effect occurs when the temperature is lowered.

These results demonstrate the trade-offs when designing the current mirrors. As a general conclusion, we can state that the cascode current mirror has better performance in terms of compliance range and output resistance with respect to the other studied current mirror topologies.

TABLE I: Simulated results for 3 values of temperature and VDD fixed in 1.5 V.

Temperature = 27 ºC			
		I_{out}	r_{out}
Simple	W=900 n	10 uA	121.21 kΩ
Current	W=1800 n	10 uA	99.70 kΩ
Mirror	W=2700 n	10 uA	90.99 kΩ
Cascode	W=900 n	10 uA	2111.16 kΩ
Current	W=1800 n	10 uA	1377.01 kΩ
Mirror	W=2700 n	10 uA	1681.11 kΩ
Wilson	W=900 n	5 uA	617.28 kΩ
Current	W=1800 n	5 uA	751.87 kΩ
Mirror	W=2700 n	5 uA	847.45 kΩ
Temperature = 0 ºC			
		I_{out}	r_{out}
Simple	W=900 n	9.63 uA	121.50 kΩ
Current	W=1800 n	9.60 uA	100.20 kΩ
Mirror	W=2700 n	9.57 uA	90.66 kΩ
Cascode	W=900 n	8.75 uA	2272.72 kΩ
Current	W=1800 n	8.99 uA	1886.79 kΩ
Mirror	W=2700 n	9.08 uA	1754.38 kΩ
Wilson	W=900 n	4.73 uA	662.25 kΩ
Current	W=1800 n	4.42 uA	793.65 kΩ
Mirror	W=2700 n	4.01 uA	1010.40 kΩ
Temperature = 70 ºC			
		I_{out}	r_{out}
Simple	W=900 n	10.55 uA	120.77 kΩ
Current	W=1800 n	10.60 uA	99.60 kΩ
Mirror	W=2700 n	10.62 uA	91.57 kΩ
Cascode	W=900 n	11.57 uA	2000 kΩ
Current	W=1800 n	11.44 uA	1754.38 kΩ
Mirror	W=2700 n	11.39 uA	1639.34 kΩ
Wilson	W=900n	7.09 uA	568.18 kΩ
Current	W=1800 n	6.52 uA	704.22 kΩ
Mirror	W=2700 n	6.32 uA	793.65 kΩ

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